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Technical Note

Ionizing radiation effects on a 64-channel charge measurement ASIC designed in CMOS 0.35 μm technology

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ABSTRACT

A 64-channel circuit Application Specific Integrated Circuit (ASIC) for charge measurement has been designed in CMOS 0.35 μm technology and characterized with electrical tests.

The ASIC has been conceived to be used as a front-end for dosimetry and beam monitoring detector read-out. For that application, the circuitry is housed at a few centimeters from the irradiated area of the detectors and therefore radiation damages can affect the chip performances.

The ASIC has been tested on an X-ray beam. In this paper, the results of the test and an estimate of the expected lifetime of the ASIC in a standard radio-therapeutical treatment environment are presented. An increase of the background current of 2 fA/Gy has been observed at low doses, whilst the gain changes by less than 3% when irradiated up to 15 kGy. Furthermore it has been assessed that, when used as an on-line beam monitor and the annealing effect has been taken into account, the background current increase is ~440 fA/year.

1. Introduction

The radiation effects on electronic devices are a complex topic, which has been studied and results have been reported in several papers [1–3]. Radiation damage mechanisms are typically classified under two main areas: *lattice displacement* and *ionization effects*. The latter, that are the most detrimental for CMOS devices, are caused by incident charged particles and by ultraviolet or X-radiation which deposits energy via ionizing mechanism into the devices.

The ionization effects can be grouped in two classes: the *Total Ionizing Dose* (*TID*) *effects* and the *Single Event Effects* (SEEs). The TID accounts for the cumulative damage of the insulation oxide caused by the ionizing radiation over the exposition time. Gradual accumulation of holes in the oxide layer in MOS transistors leads to worsening of their performances, up to the device failure when the dose is high enough [1]. The SEEs are changes in the device caused by a single particle, which can induce glitches and soft errors and can lead to the destruction of the device if they trigger other damage mechanisms, e.g. a latch-up [2,3].

Performances of microelectronic devices working in a relatively large radiation background are expected to deteriorate as a function of the total dose in a way which is not easily predictable from any other experiments or models, but only a direct measure can provide the necessary information.

In this paper we report about a measurement of the TID effects on an Application Specific Integrated Circuit (ASIC) (known as Tera07) which has been developed by our group for radio-therapeutical uses.

Tera07 is an improved version of a multi-purpose integrated circuit to read-out detectors for dosimetry and beam monitoring [4]. Details on the chip, a 64-channel ASIC, can be found in Ref. [5].

Each channel is based on a current-to-frequency converter followed by a counter. The converter can integrate currents of both polarities. Whenever the integrator output voltage crosses a comparator threshold two actions are taken: a given charge quantum is subtracted from the input and a pulse is counted by a synchronous 32-bit up/down counter. The frequency of the pulses is thus proportional to the input current. The ASIC is designed to work at a clock frequency of 100 MHz and with a maximum output frequency of 20 MHz. A detailed description of a channel,

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the architecture of the chip, and the performances are reported in Refs. [5,6].

Tera07 has been designed in a commercial CMOS 0.35 μm technology, while previous versions were implemented in CMOS 0.8 μm. The decrease of the gate size and oxide thickness as well as the improvement of the interface quality results in a strong reduction of the radiation-induced trapped charges [7,8].

A radiation damage study has been done by testing a few chips on an X-ray beam facility (SEIFERT RP149) at CERN. With this test we address the damage due to X-ray effects essentially in the oxide. As previously discussed, interactions with other types of particles, such as hadrons, can cause atom displacement from the lattice or SEE-inducing phenomena like latch-up and logic states flipping [9]. These effects are not part of the test reported here. In fact we focused the measurements to the circumstantial radio-therapeutical applications. In this practice, a low-energy X-ray background is expected to irradiate the electronics and in particular the ASIC chip hosted inside the case. The leaks through the collimator and the large-angle scattering of the primary radiation in the phantom are the sources of the X-ray background to the ASICs. In Fig. 1 the layout of the front-end electronics for a typical radio-therapeutical application is sketched (see Refs. [10,11] for a detailed description): the ASICs are located at a few centimeters from the active area of the detector. The impact of the background at the ASIC level can be estimated with usual dosimeters and it depends on the specific setup, namely the linear accelerator and collimator type.

The paper is organized as follows: in Section 2 the experimental setup of the test is described, while in Section 3 the test results are reported. In Section 4 the impact of the delivered dose on the chip performances for typical on-line operations is discussed. Conclusions are drawn in Section 5.

2. Experimental setup

The measurement of the X-ray beam damage on a chip can be done with or without the case protection.

In the first approach it is possible to derive directly the relationship between delivered dose and effect on the electronic devices, while the latter is more focused on the effects of the delivered dose on the final system. Indeed for the end-user the relevant measurements are those performed with a conceivable final setup. For this reason, to employ directly the test results in a typical radio-therapeutical application of the chips the radiation damage has been measured with the case.

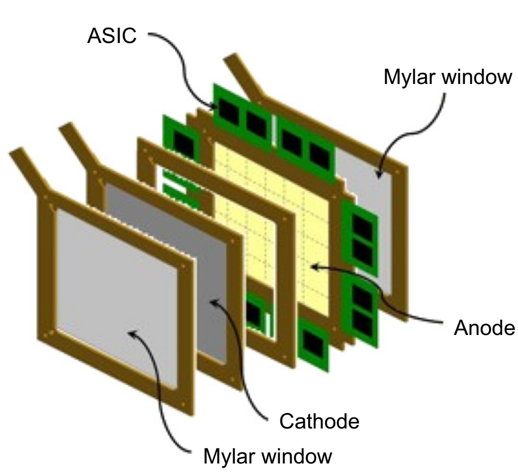

Fig. 1. Exploded view of the pixel detector described in Ref. [10]: the location of the ASICs is shown.

One of the most fruitful applications of the Tera chips is their use as front-end in 2D detectors for the measurement and characterization of therapeutic photon or electron beams as in the *I'mRT MatriXX* [12] device. For such applications, the amount of leakage radiation to where the chips are positioned depends on the setup, primarily the collimator. Furthermore, the leakage dose, mainly due to soft photons with energy of the order of tens of keV, can be directly measured.

The maximum voltage of the X-ray tube used in this test is 60 kV. The generated photons have been filtered by a 100 μm Al window to cut off the low-energy spectrum ($\leqslant$10 keV) and finally collimated to match the chip surface. The dose rate, up to 4 kGy/min, can be controlled via the tube current. The calibration of the machine has been done using a PIN diode at 16 cm from the X-ray exit collimator. For the test the chips have been placed at the same distance of 16 cm from the collimator. The tube voltage has been set to 50 kV and the dose rate in a range between 50 and 100 Gy/min.

The chip, occupying an area of $(5.4 \times 4.5)\,mm^2$, was enclosed in a ceramic (Al_2O_3 min. 90%, density = $3.7\,g/cm^3$) package with a cover 1.65 mm thick. The dose effectively transmitted through the case has been evaluated with the Electron Gamma Shower (EGS) Monte Carlo [13,14]. We found that only ~78% of the photon energy as measured at the case surface is then transmitted through the case itself and reaches the chip. However, throughout the paper we quote the delivered dose at the case rather than the one to the chip.

The test was a sequence of the following operations: (a) exposure of the chip to a given dose, followed by (b) the measurements of the background current and the charge quantum.

During the irradiation the ASICs have been powered and clocked. For this purpose the chips have been mounted on a socket housed in the irradiation test motherboard (so-called IRR-Board). In Fig. 2 the experimental setup used during the irradiation is sketched.

To acquire data a system based on a National Instrument PCI DAQ card (PCI 6533) and the LabVIEW software has been used [15,16]. The performances of the channels have been studied using a Keithley 2400 voltage generator. It provides precision voltage in the range between 1 μV and 211 V with an accuracy of 0.012%.

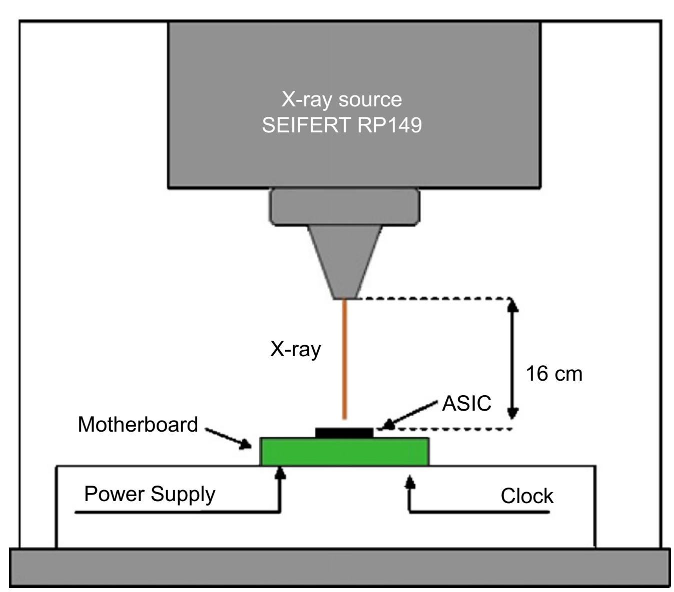

Fig. 2. Sketch of the irradiation setup used at the CERN facility to characterize the ASIC.

The voltage, via a 10 MΩ resistor, supplies the current injected into the channel. During these tests the chips have been mounted in a socket that is housed on the test board (so-called *TestBoard-TERA07*).

The main function of the board is to adapt the ASIC voltage levels and line topology to the PCI DAQ card. A detailed description of TestBoard-TERA07 is presented in Ref. [5].

To assess the degradation of the chip performances, measurements of the background current and charge resolution were repeated as a function of the delivered dose up to 15 kGy. The full procedure was completed in a day.

3. Test and results

The ASIC has been previously characterized (see [5]) by measuring:

- background currents;
- effective gain for different charge quanta;
- linearity of the current-to-frequency converter.

The background current is less than 500 fA with a mean value of 230 fA, while the spread (r.m.s.) of the charge quantum is 4.3% for a gain of 50 fC and less than 1% for 350 fC. The ASIC has a very good linearity for both positive and negative currents over a current input dynamic range of four orders of magnitude, from 500 pA to 3 μA.

The radiation damage studies discussed in this paper address the total dose effects on the ASIC performances and the recovery effect.

To study the total dose effects the chips have irradiated in several dose steps up to 15 kGy. After each irradiation, the following parameters have been measured for charge quanta of 50, 100, and 200 fC, hereafter referred as reference settings:

- the counts due to background current, corresponding to open input;
- the gain.

For a typical channel, the background current is shown in Fig. 3 as a function of the integrated delivered dose. Fig. 3 shows that, independently of the charge quantum, the pedestals increase with the integrated dose. As an example, for a given channel with the charge resolution set to 50 fC, a background of 250 fA has been measured before irradiation, which increased to 150 pA at 15 kGy. The background current is almost independent of the charge quantum: this indicates that the capacitor values are not affected by the radiation.

After each irradiation the charge quantum has been measured for both polarities. Therefore, the charge quantum distribution has been measured for the reference quanta settings and for both positive and negative polarities.

In Fig. 4, for a typical channel we show the charge quantum distribution versus the integrated delivered dose for three different *Q* values: 50 fC in (a), 100 fC in (b), and 200 fC in (c). We remark that the differences between design and experimental gain values are explained by the spread of the capacitance values for this technology (±10%). The measured charge quantum increases with the dose for positive currents (dots) and decreases for negative ones (square). This is consistent with the fact that the measured background current is negative and its absolute value increases with the irradiation. In fact, for a positive input current the effect of the negative leakage is to decrease the net current and therefore appears as a reduction of the gain (and thus as an

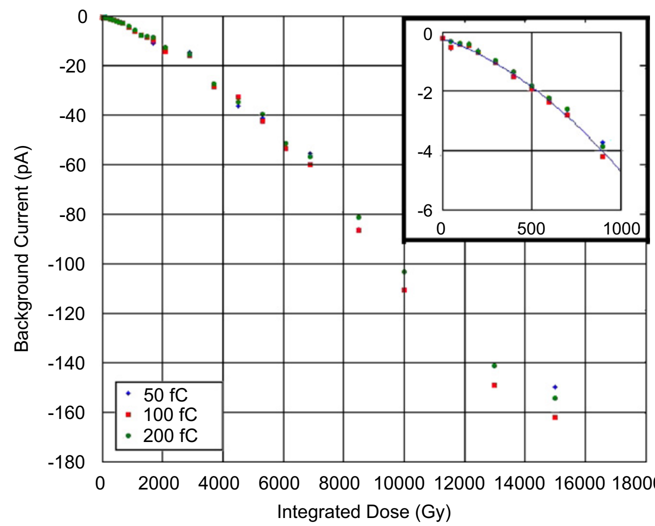

Fig. 3. Background current as a function of the integrated X-ray dose for different charge quanta; the inset shows the trend for doses up to 0.8 kGy. Statistical uncertainties are within the dimension of the symbols.

increase of the charge quantum). For negative currents the effect is reversed, thus leading to a decrease of the charge quantum of the same quantity. Over a range of 15 kGy the deviation of the gain for both positive and negative input currents with respect to the average value is less than 10% for 50 fC and 3% for 200 fC. It should be noted that the above deviations can be easily corrected for with the standard periodical gain calibration. Indeed the data show that the radiation damage effects are limited to the background current, which increases almost linearly and becomes three orders of magnitude bigger for an integrated dose of 15 kGy.

However, it is known that in silicon devices time and temperature can trigger a self-recovery process, which is known as *annealing*. In short, the net effects of the irradiation result in an accumulation of holes which remain trapped in the oxide near the SiO_2–Si interface that with time tend to decrease. Two phenomena are the base for the explanation: a tunnel-effect-based annealing originates the recombination of the electrons into the trapped holes [17,18] and a thermal annealing for which electrons escape the valence band and recombine with the holes.

The self-recovery process has been studied as a function of time after irradiation. For this study the value of the background current and the charge quantum have been measured at regular time intervals. The self-recovery effect is shown in Fig. 5: the background current for a typical channel is plotted as a function of the number of days after the irradiation. A measurement of the background after ~1.5 years shows that the recovery is not complete and a background current of 12 pA remains after the annealing process is saturated. From the distribution of the experimental points we infer the hypothesis that two processes play a significant role in the overall neutralization of the holes trapped close to the SiO_2–Si interface. The recovery can be described by the sum of two exponential trends, which account for a short- and a long-term annealing, and an asymptotic saturation, A_3, fixed by the measurement to 12 pA:

$$I(t) = A_1 \exp(-t/\tau_1) + A_2 \exp(-t/\tau_2) + A_3 \quad (1)$$

By fitting the experimental points to Eq. (1), it was found that τ_1~8 days and τ_2~41 days. This indicates that two annealing processes compete with each other: a faster one having a time constant of ~8 days and a slower mechanism with a much larger time constant. These two processes may correspond to the tunnel effect base and the thermal annealing. In Fig. 5 the fit result, $I(t)$, is

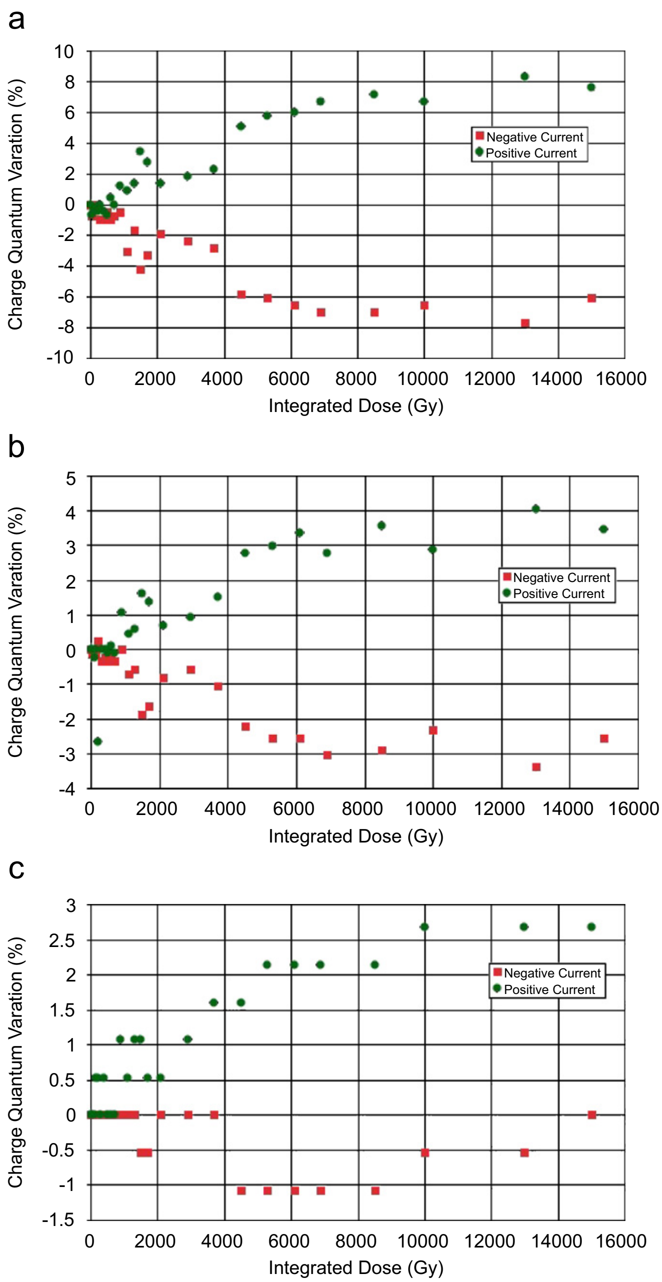

Fig. 4. (a) Charge quantum variation as a function of the integrated X-ray dose for a nominal charge quantum of 50 fC. Statistical uncertainties are within the dimension of the symbols. (b) Charge quantum variation as a function of the integrated X-ray dose for a nominal charge quantum of 100 fC. Statistical uncertainties are within the dimension of the symbols. (c) Charge quantum variation as a function of the integrated X-ray dose for a nominal charge quantum of 200 fC. Statistical uncertainties are within the dimension of the symbols.

reported (full line) together with the exponential curves (dashed lines), showing both fast and slow component. The annealing saturation leaves a background current, which is reported as a dash–dotted line.

A second chip irradiated with a total dose of 6.9 kGy showed similar trends.

4. Discussion

It is worthwhile to discuss in more detail the interplay between damage and self-recovery: in general the topic is rather complex, but when limited to a specific case some conclusions can be drawn. The following analysis is focused on an application where the chips are used to monitor on-line therapeutic treatments with photon or electron beams: in this case each single field delivery to a patient is monitored, resulting in a very intensive use of the detector. This is a worst case with respect to the use of the ASICs for Quality Assurance (QA) of the beam and for the treatment planning: in this respect the detector is used typically once per day and the amount of irradiation is at least an order of magnitude smaller.

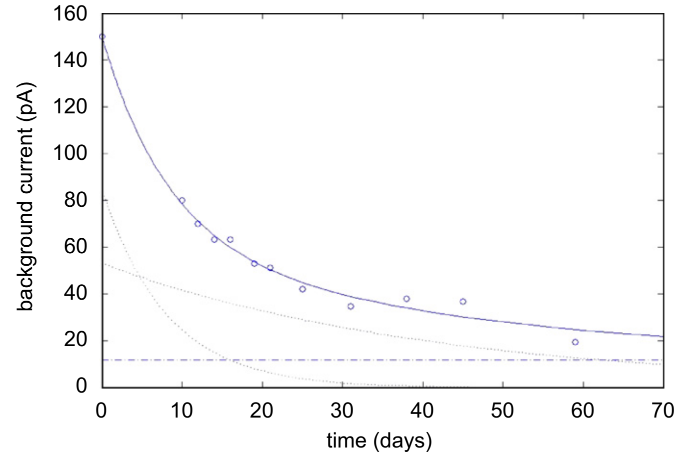

Fig. 5. Absolute value of the background current for a charge quantum of 50 fC as a function of time after an integrated X-ray irradiation of 15 kGy: the continuous line shows the function described in Eq. (1) with $\tau_1 = 8$ days and $\tau_2 = 41$ days. The dash–dotted line shows the annealing saturation as measured after 1.5 year. Statistical uncertainties are within the dimension of the symbols.

To evaluate the expected dose delivered to a chip during the treatment the following assumptions have been made:

- A typical standard treatment fraction is designed to deliver 2 Gy to the patient target.
- A conservative estimation of the fraction of the dose to the ASIC is 1%. This figure is substantiated by several measurements with different setups.
- The average number of patients per day is 100 corresponding to a total delivered dose to the ASICs of 2 Gy/day (100 patients $\times$ 2 Gy/patient $\times$ 0.01).
- The treatment session lasts for 12 h during the day.
- The total number of treatment days per year is 260, divided into 52 weeks of 5 working days.

Taking into account the above assumptions, it can be estimated that the detector-sensitive area will receive an integrated dose of 52 kGy/year, while the ASIC will receive a dose of 520 Gy/year.

To study the impact of the radiation damage taking into account the self-recovery effect, the background current I_{bckg} can be modeled as a result of the product of two functions. The first function is a parameterization of I_{bckg} as a function of the dose D: ($I_{bckg0}+aD+bD^2$), where I_{bckg0} is the background current before the dose D has been delivered, $a = 2$ fA/Gy and $b = 2.5 \times 10^{-3}$ fA/Gy^2 are the linear and quadratic term, respectively. I_{bckg0}, a and b have been derived from Fig. 3 by fitting the low-dose inset ($D < 1.6$ kGy) of the plot to a quadratic curve. The second function is Eq. (1): we assume that, after the annealing occurs, the background current saturates to a value which scales linearly with the total dose. The model included the expected time sequence: 52 weeks, each with 5 working days dedicated to treatments during 12 h.

After 1 year of operations the expected background current increases by ~440 fA from ~230 to ~670 fA. Based on the above

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figure it is possible to conclude that the effect of the radiation damage on the background current is marginal and, on the other hand, the effect on the gain can be easily taken into account by the routine periodic calibration.

5. Conclusions

An ASIC in CMOS 0.35 μm technology has been developed to be used as front-end electronics for the read-out of multi-channel detectors. The 64-channel chip is a charge measurement circuit: the quantization error (charge quantum) can be selected in the range between 25 and 1155 fC for a maximum input current of 3 μA. The background current (open input) is ~230 fA.

The ASIC can fit many applications; it has already been used for the read-out of several types of detectors [10–12].

In a typical application the front-end electronics is housed at a few centimeters from the irradiation area of the detectors: for this reason we have studied the radiation damage to the ASIC due to soft photon irradiation.

From the performed test it has been found that the background current increases almost linearly with a rate of 2 fA/Gy for low absorbed dose (up to ~100 Gy) and quadratically for larger doses. The charge quantum changes as a function of the delivered dose up to 15 kGy within 10% for 50 fC down to 3% charge for 200 fC.

The self-recovering process and its effect on the background current have been studied; it can be represented by the sum of two exponential functions: a short term with time constant of 8 days is followed by a slower process with a time constant of 41 days. However, the annealing process shows a saturation effect and a background current remains even after many time constants. From these measurements it is possible to conclude that by using the detector as on-line beam monitor and inferring typical operation conditions the background current would increase by ~440 fA/year. However, this figure is still at least three orders of magnitude smaller than the expected current range for typical measurements.

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References

[1] T.P. Ma, Paul V. Dressendorfer, Ionizing Radiation Effects in MOS Devices and Circuits, Wiley-IEEE, ISBN 047184893X, 1989.
[2] P.S. Winokur, Ionizing Radiation Effects in MOS Devices and Circuit, Wiley, New York, ISBN 047184893X, 1998.
[3] Di Cor L. Claeys, Eddy Simoen, Technology & Industrial Arts (2002).
[4] A. La Rosa, et al., Nucl. Instr. and Meth. A (2008).
[5] A. La Rosa, et al., Nucl. Instr. and Meth. A 583 (2007) 461.
[6] G. Mazza, et al., IEEE Trans. Nucl. Sci. NS-52 (4) (2005) 847.
[7] M. Campell, et al., Nucl. Instr. and Meth. A 473 (2001) 140.
[8] G. Anelli, Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technologies for the LHC experiments, Ph.D. Thesis, Institut National Polytechnique de Grenoble, France, December 2000, also available at 〈http://www.cern.ch/RD49〉.
[9] Di Len. Adams, Holmes-Siedle, Andrew Holmes-Siedle, Handbook of Radiation Effects, Oxford University Press, ISBN 019850733X, 2002.
[10] A. La Rosa, et al., Nucl. Instr. and Meth. A 565 (2006) 833.
[11] N. Givehchi, et al., Nucl. Instr. and Meth. A 572 (2007) 1094.
[12] Information about the product can be found at the web page 〈http://www.scanditronix-wellhofer.com/I_mRT_MatriXX.957.0.html〉.
[13] W.R. Nelson, H. Hirayama, D.W.O. Rogers, The EGS4 Code System, Report SLAC-265, Stanford Linear Accelerator Center, Stanford, CA, 1985.
[14] D.W.O. Rogers, Nucl. Instr. and Meth. 227 (1984) 535;
D.W.O. Rogers, Nucl. Instr. and Meth. A 227 (1984) 535.
[15] Information about the product can be found at the web page 〈http://sine.ni.com/nips/cds/view/p/lang/en/nid/201912〉.
[16] Information about the product can be found at the web page 〈http://www.ni.com/labview〉.
[17] H.E. Boesch Jr., F.B. MCLean, IEEE Trans. Nucl. Sci. NS-32 (6) (1985) 3940.
[18] P.J. McWhorter, et al., IEEE Trans. Nucl. Sci. 37 (6) (1990) 1682.

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